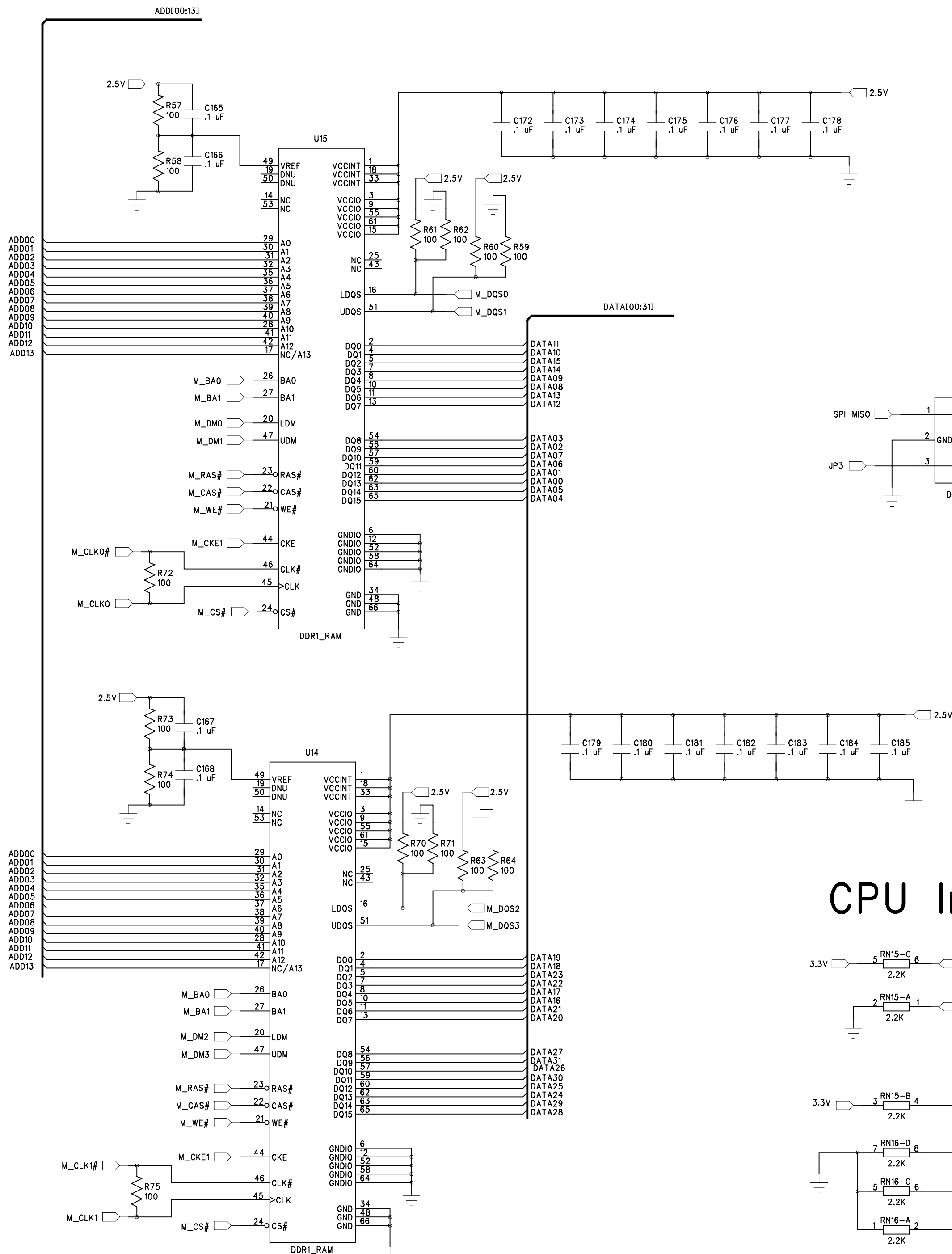
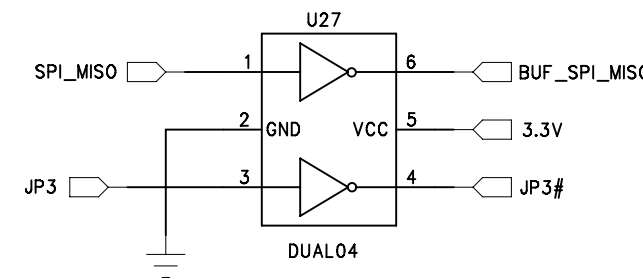
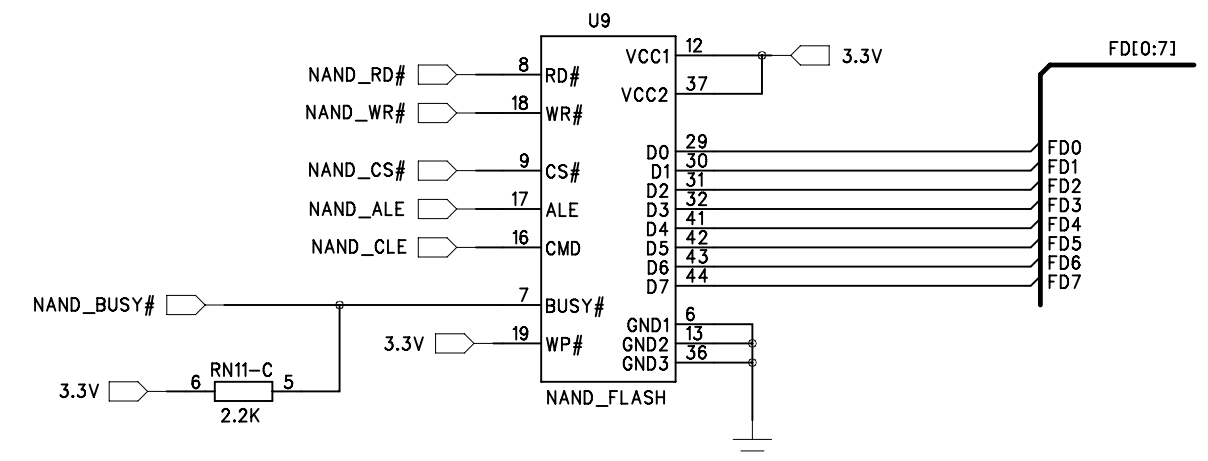


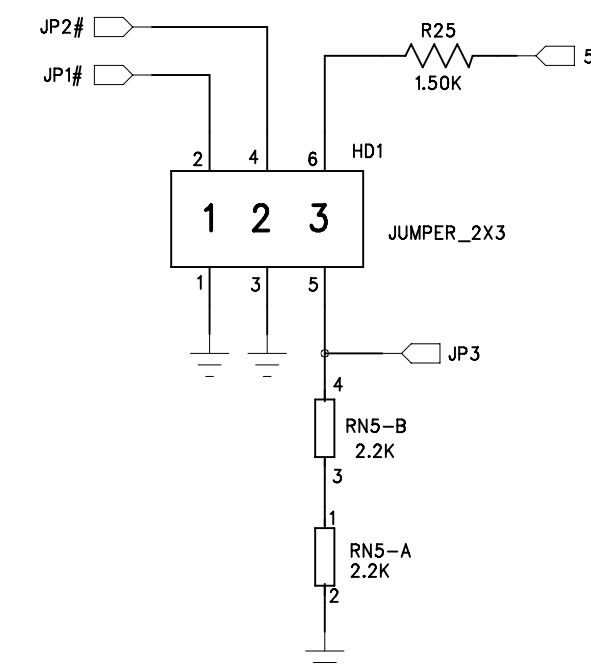
# DDR1 SDRAM



# NAND Flash

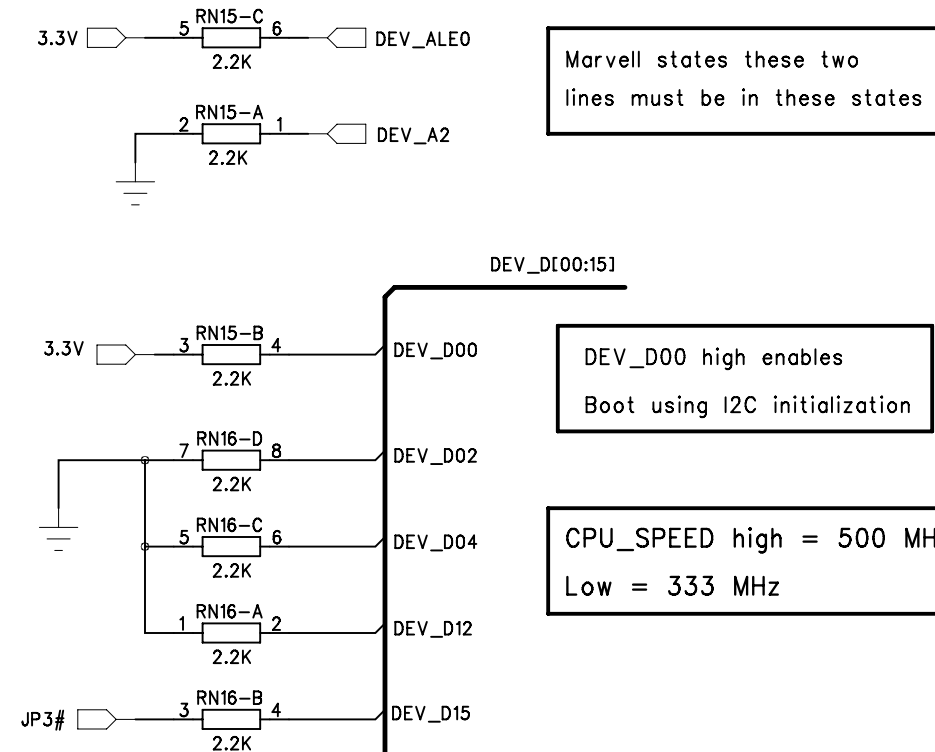


# Jumpers



JP1 = Fast Boot to NAND Flash  
 JP2 = Enable console on COM1  
 JP3 = CPU Speed is 333 MHz

# CPU Initialization

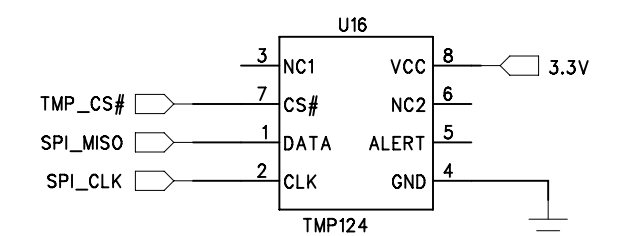


Marvell states these two lines must be in these states

DEV\_D00 high enables Boot using I2C initialization

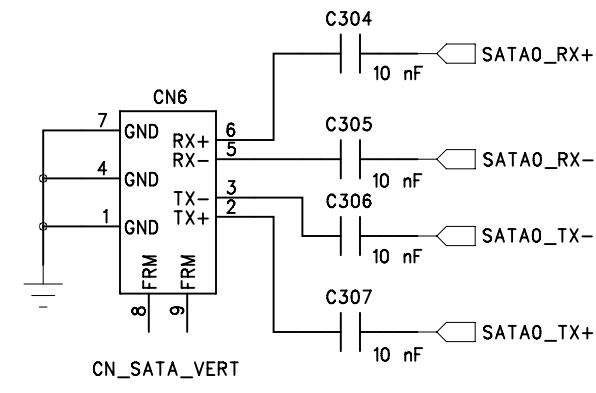
CPU\_SPEED high = 500 MHz  
 Low = 333 MHz

# Temp Sensor

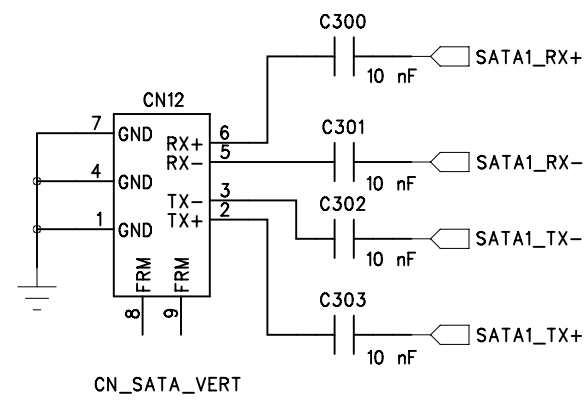


Technologic Systems	Date Jan. 28, 2008
Title: TS-7800	DDR RAM Flash
Rev:	Designer
	Sheet 2 of 8

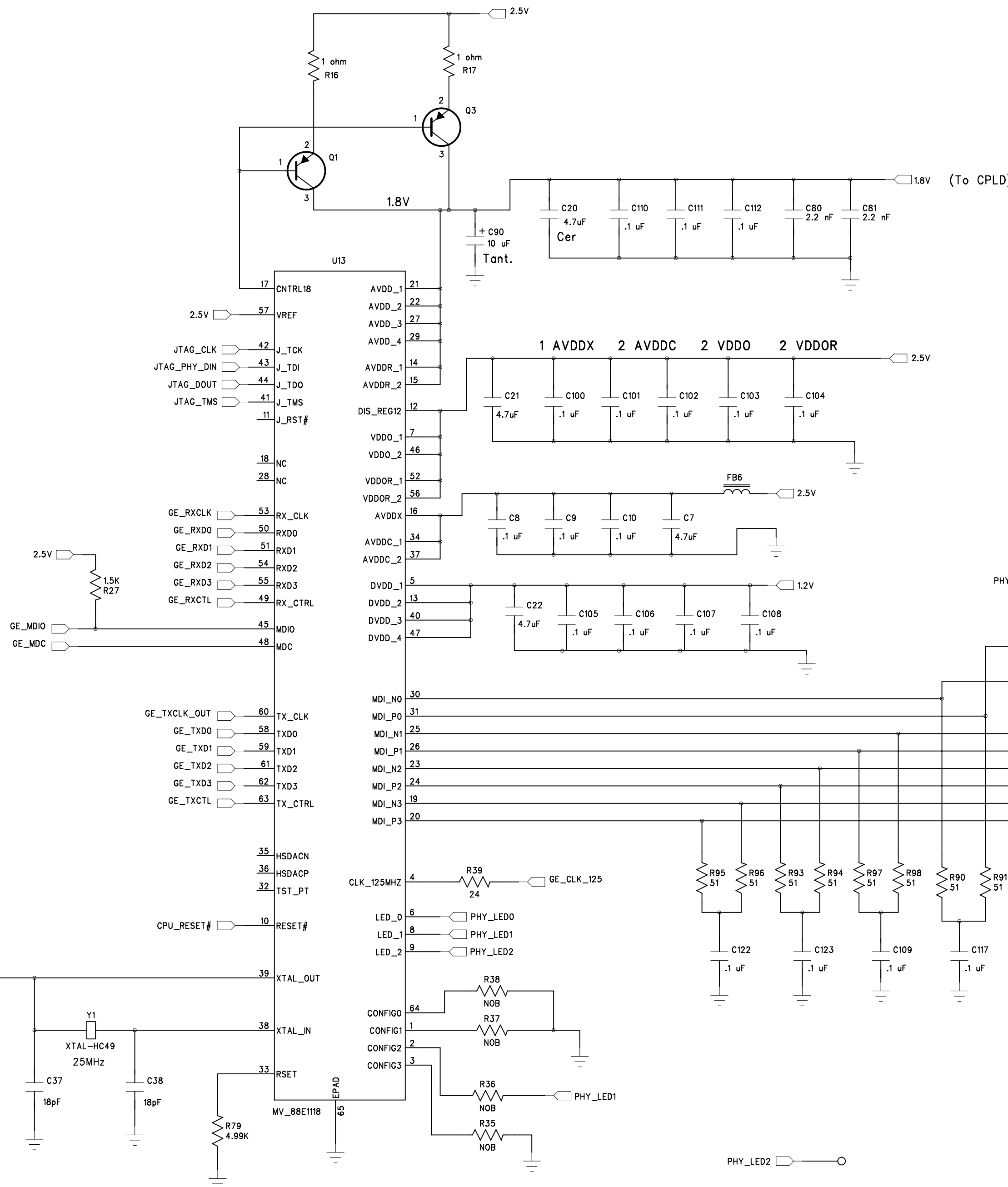
# SATA 0



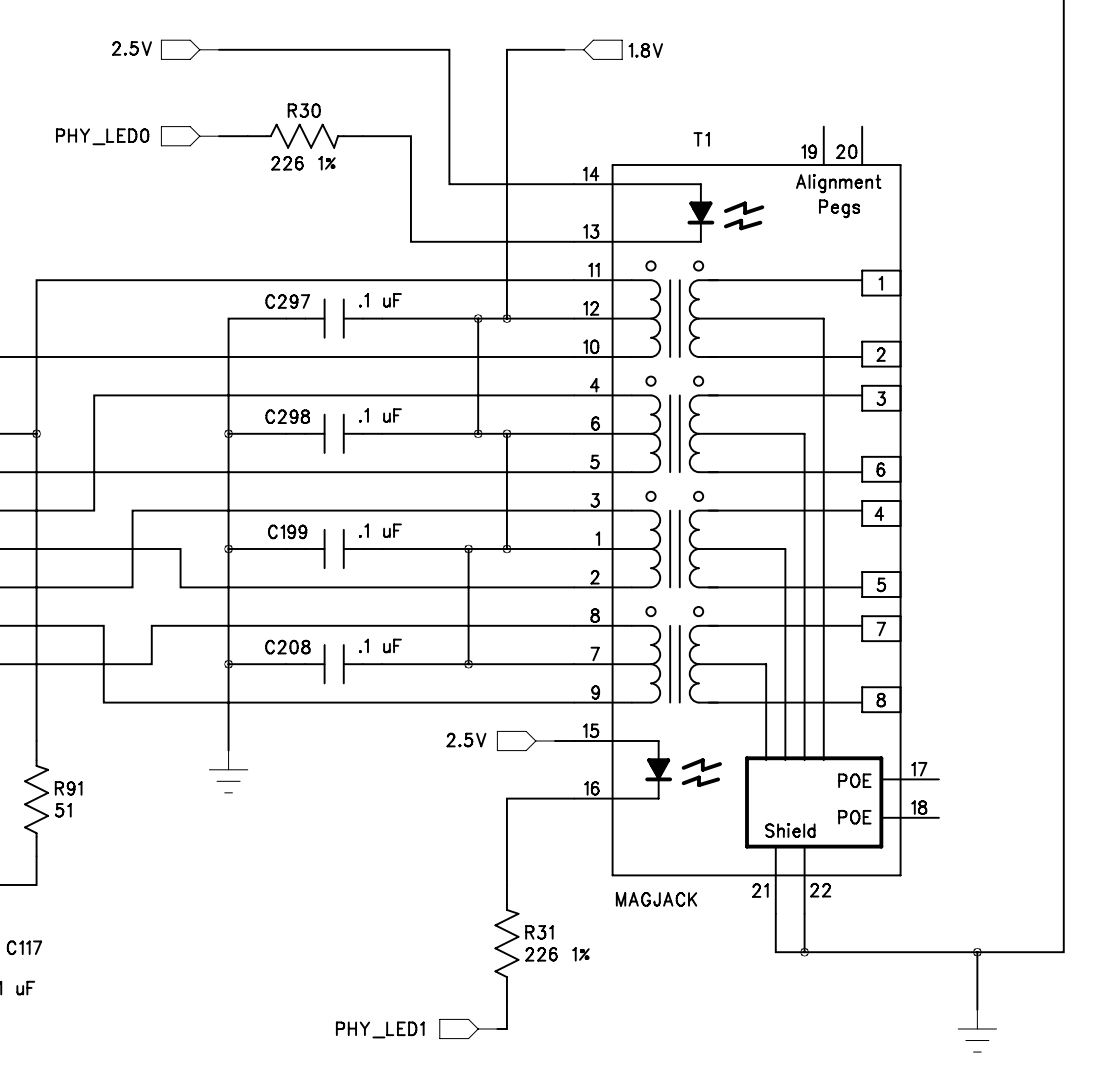
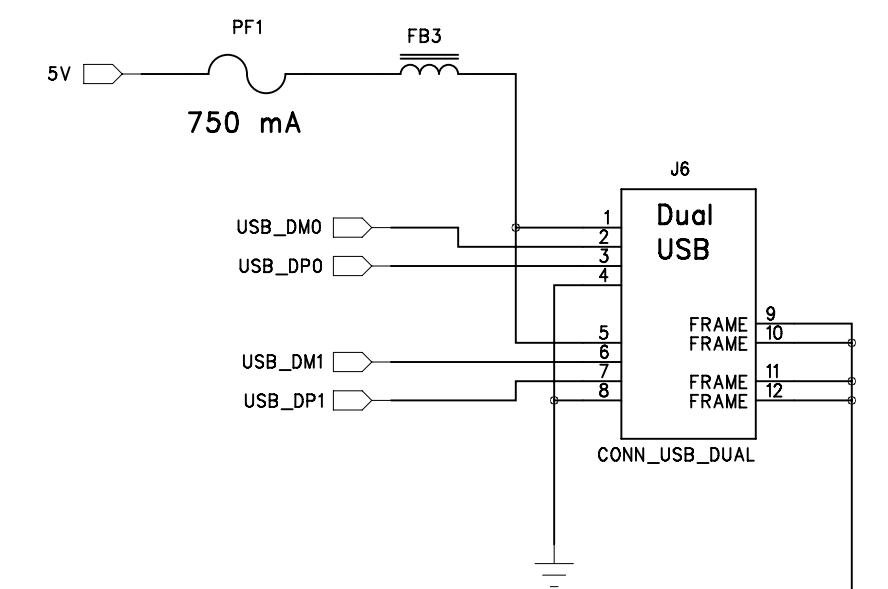
# SATA 1



# 10/100/1000 Ethernet



# USB Ports

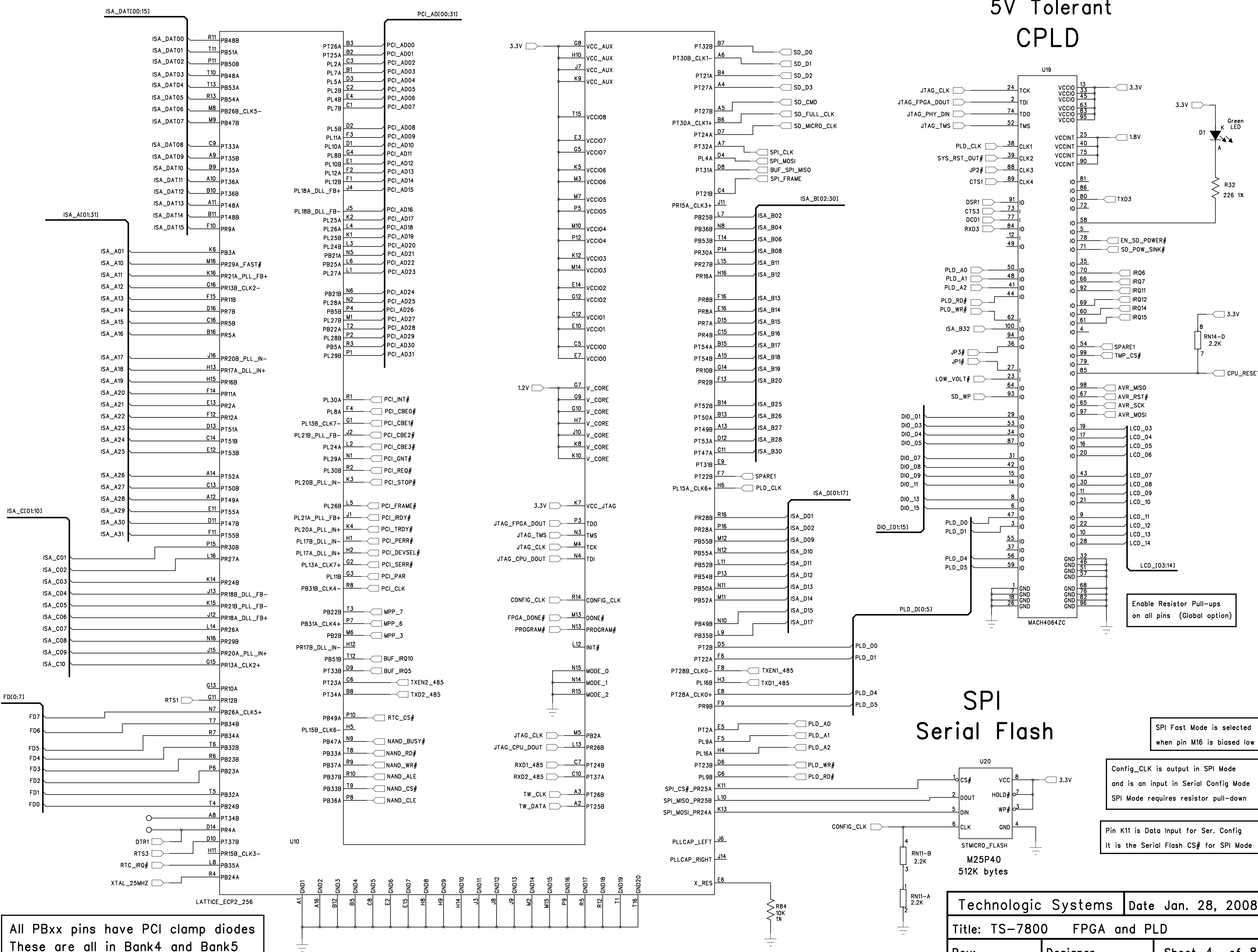


(To FPGA)

XTAL\_25MHZ

Technologic Systems	Date Jan. 28, 2008
Title: TS-7800 Ethernet, USB, SATA	
Rev:	Designer RLM Sheet 3 of 8

# 5V Tolerant CPLD



All PBxx pins have PCI clamp diodes  
These are all in Bank4 and Bank5

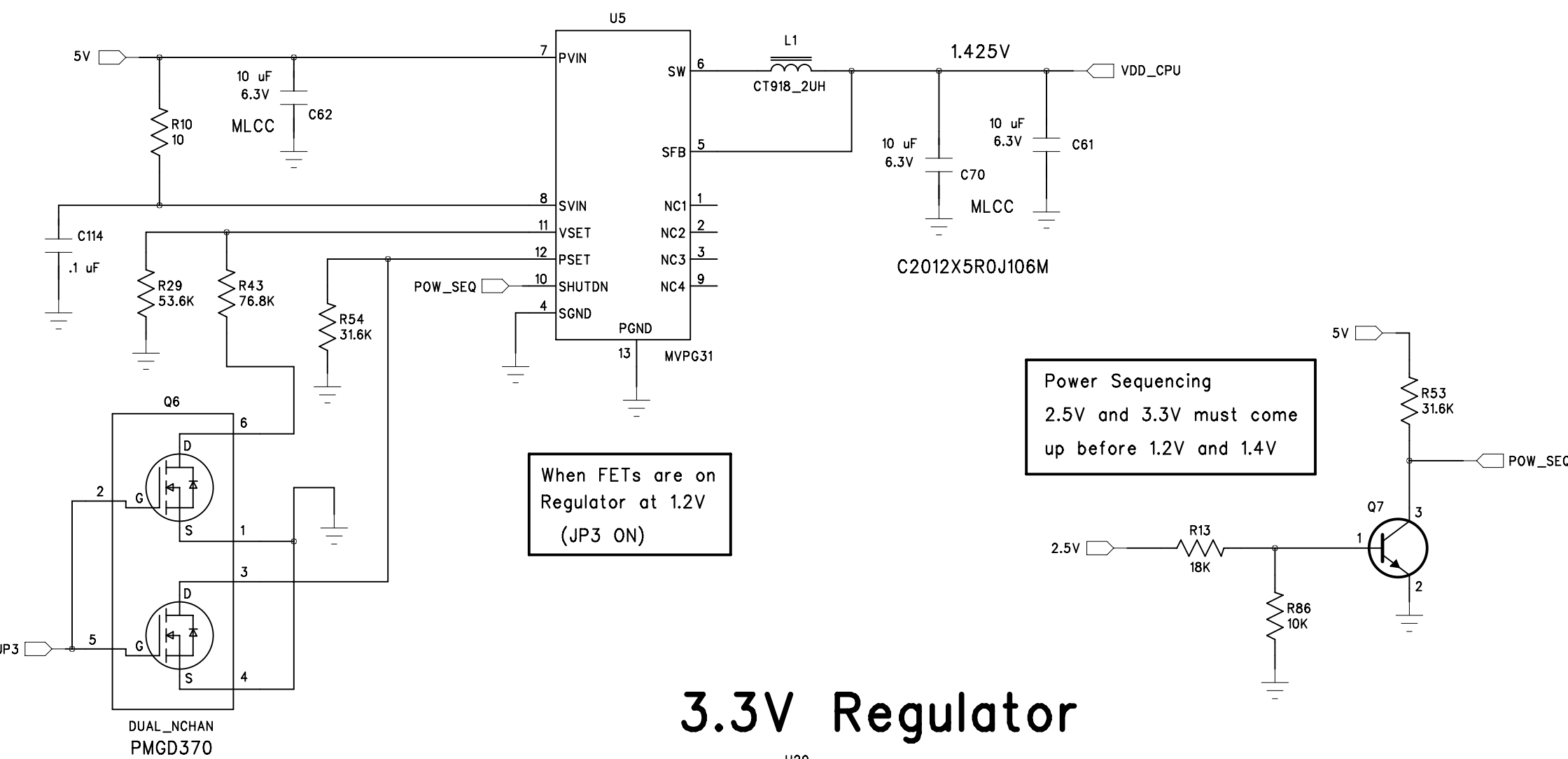
Enable Resistor Pull-ups  
on all pins (Global option)

SPI Fast Mode is selected  
when pin M16 is biased low

Config\_CLK is output in SPI Mode  
and is an input in Serial Config Mode  
SPI Mode requires resistor pull-down

Pin K11 is Data Input for Ser. Config  
It is the Serial Flash CS# for SPI Mode

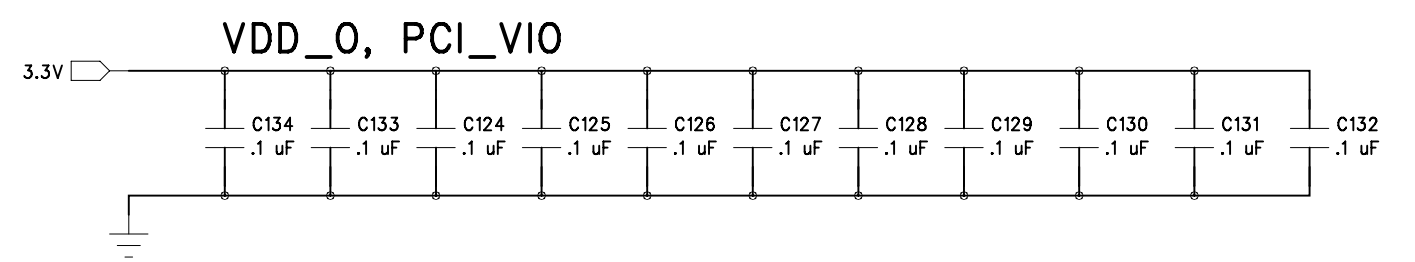
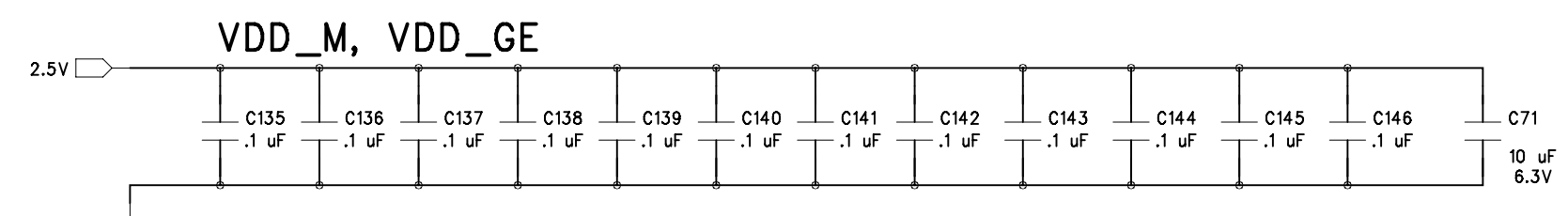
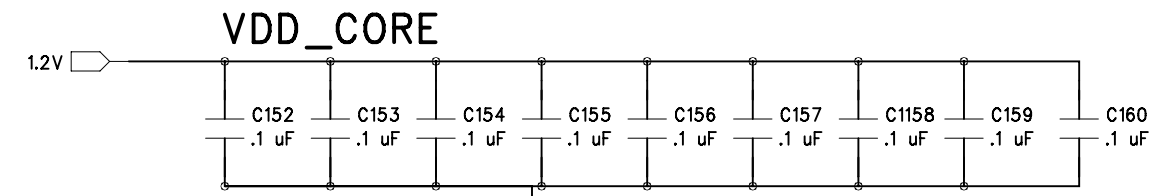
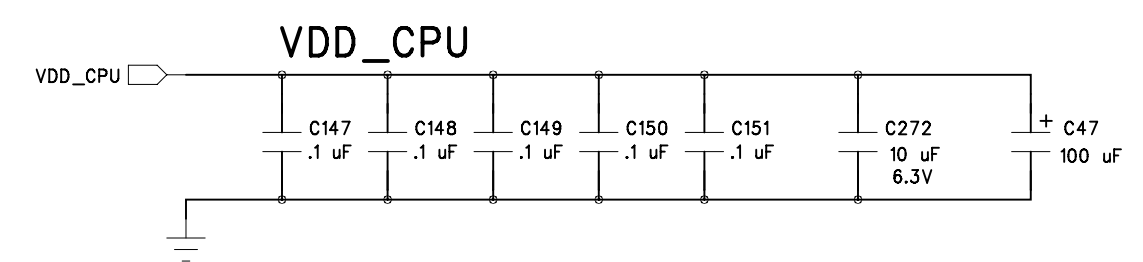
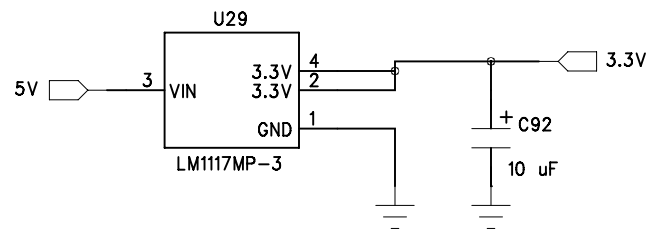
# 1.2V or 1.42V Power Supply



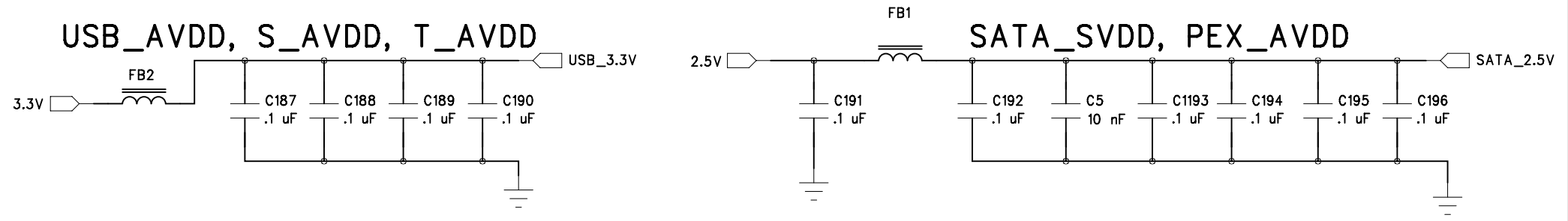
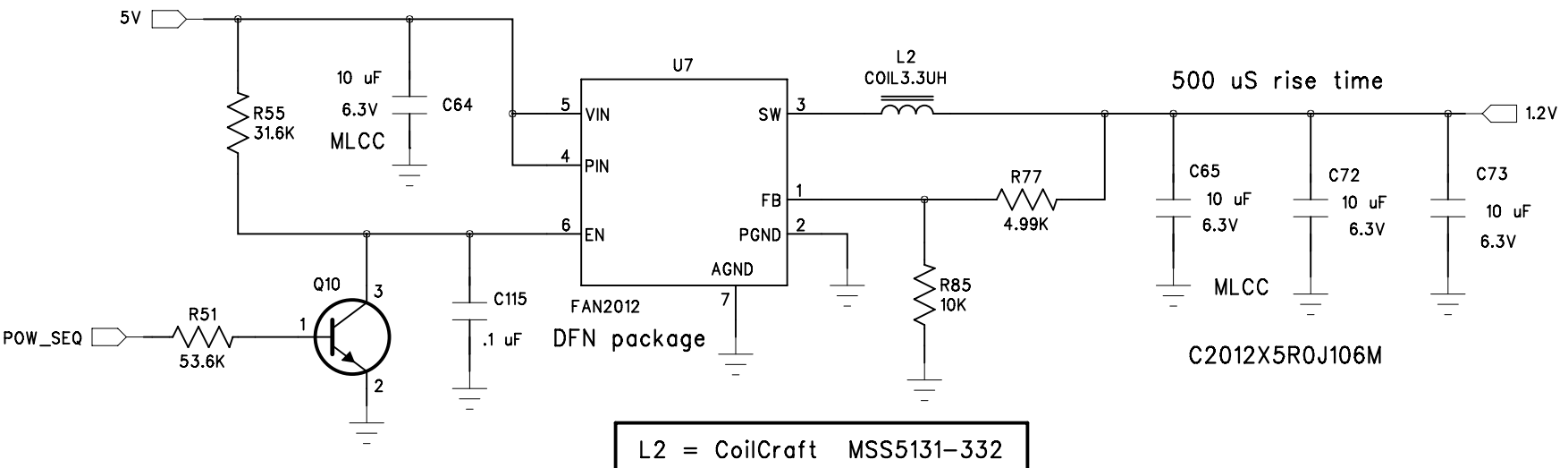
When FETs are on Regulator at 1.2V (JP3 ON)

Power Sequencing  
2.5V and 3.3V must come up before 1.2V and 1.4V

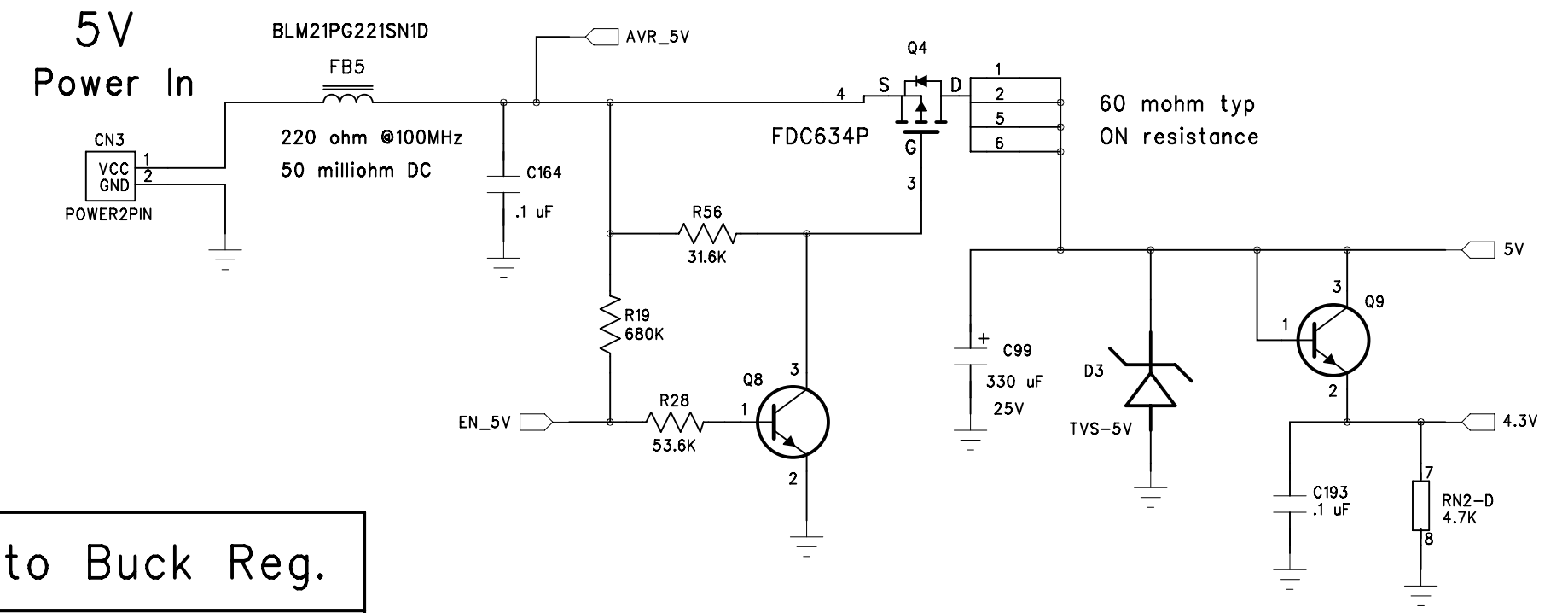
## 3.3V Regulator



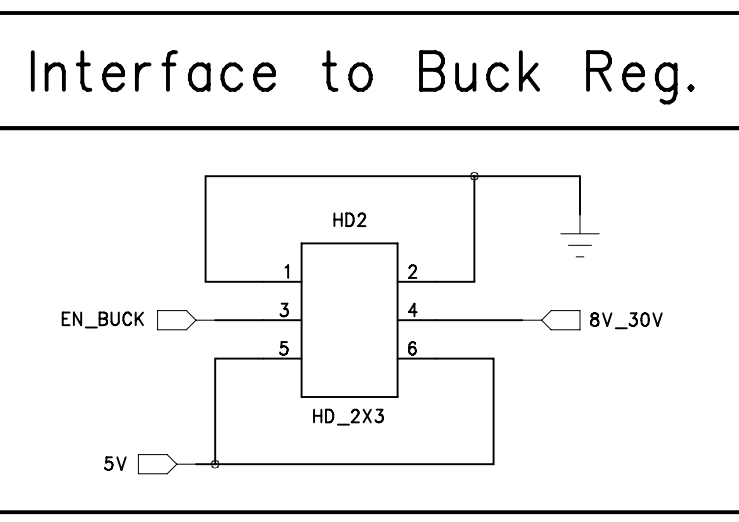
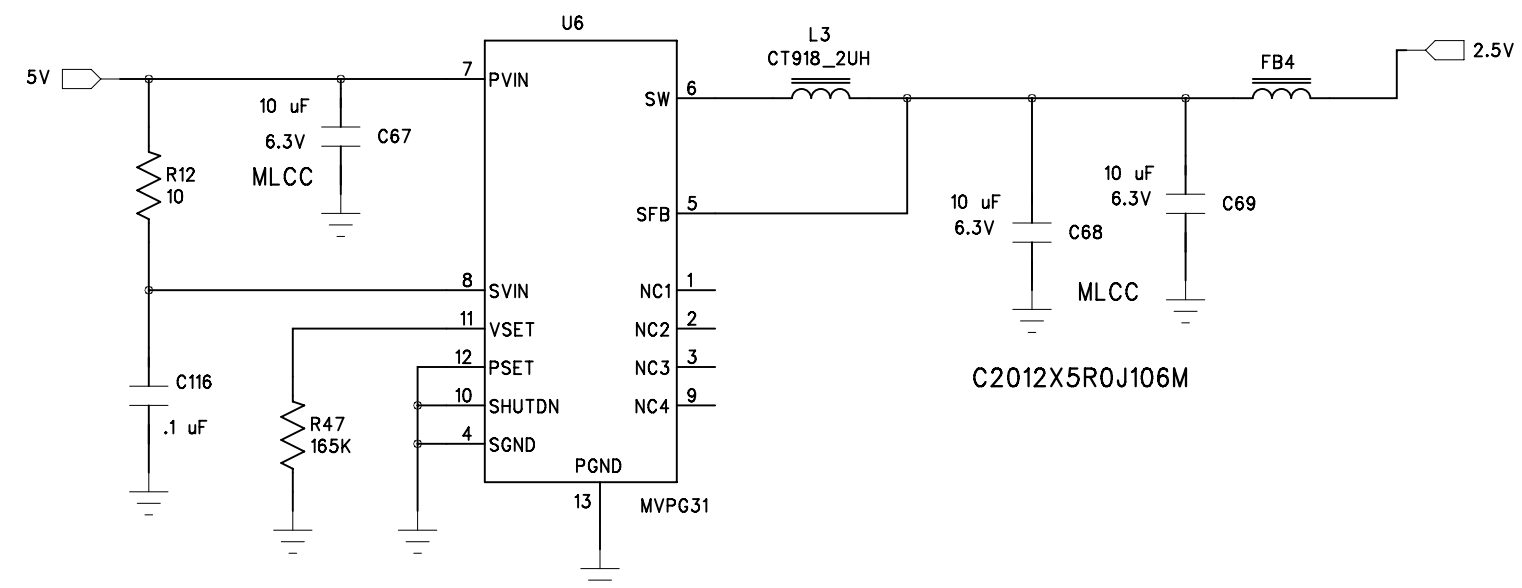
## 1.2V Power Supply up to 1500 mA



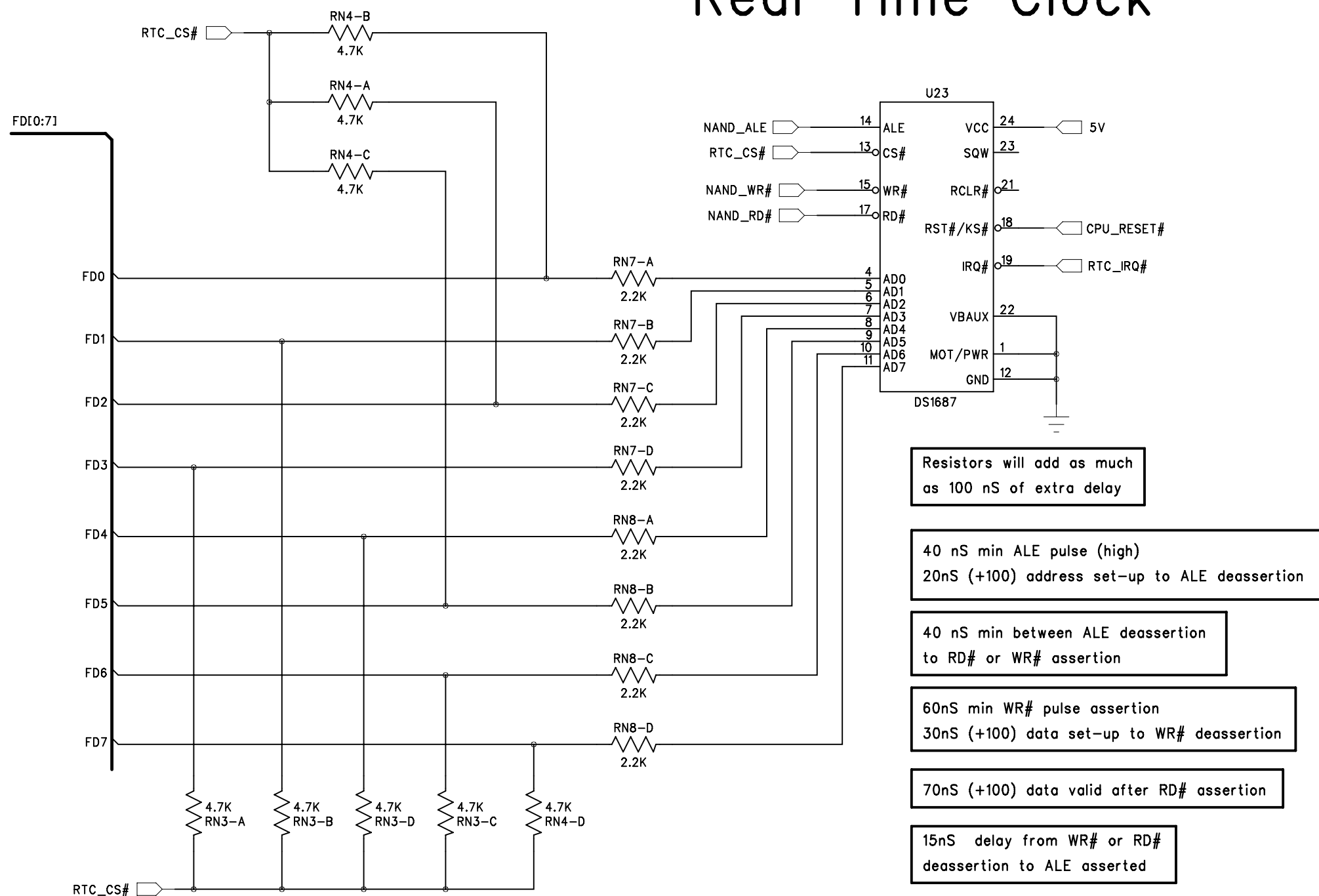
## 5V Switch



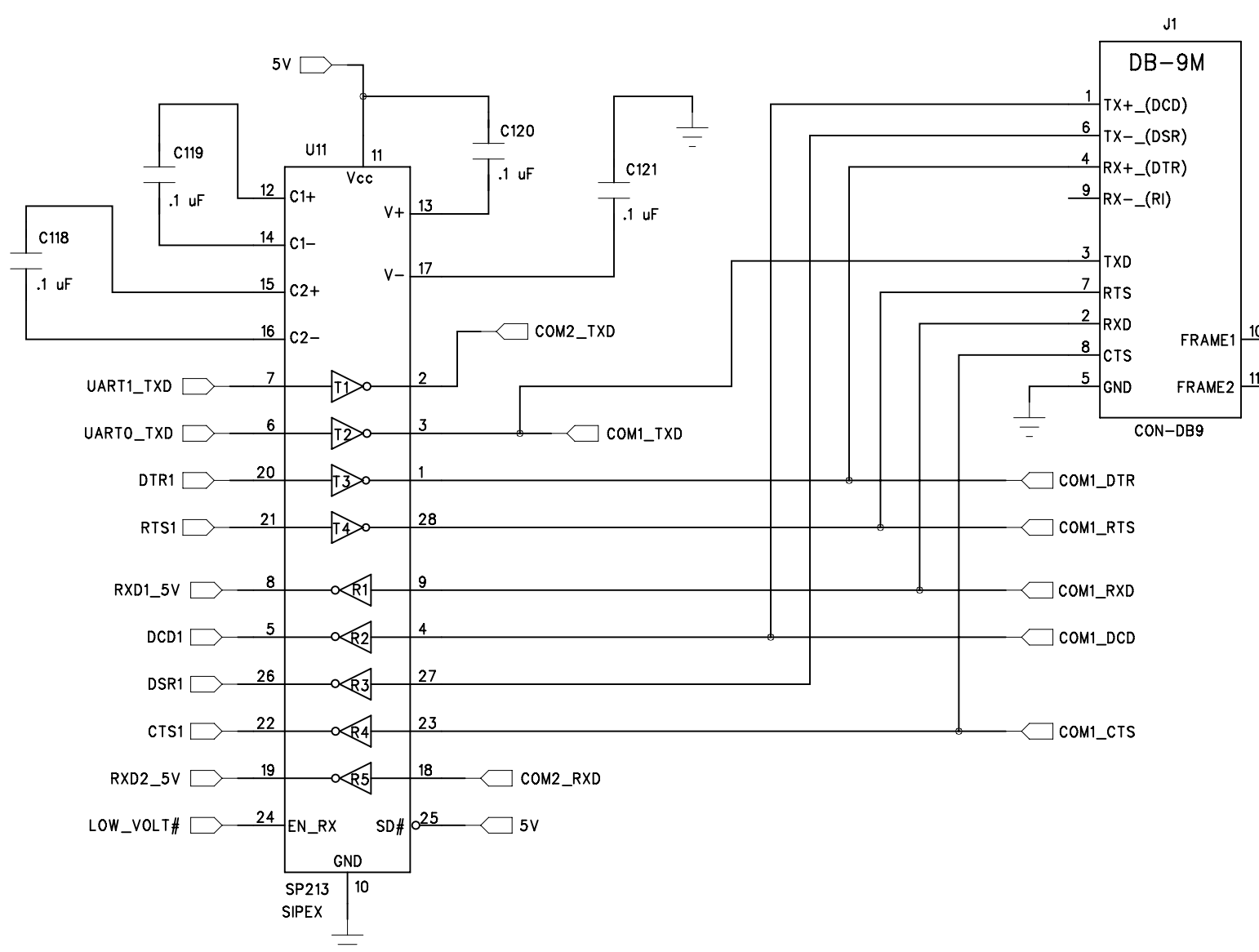
## 2.5V Power Supply



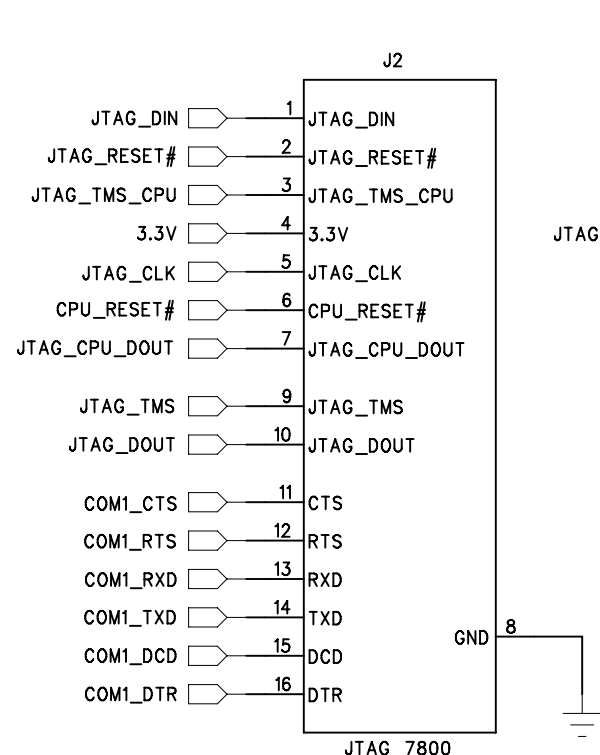
# Real Time Clock



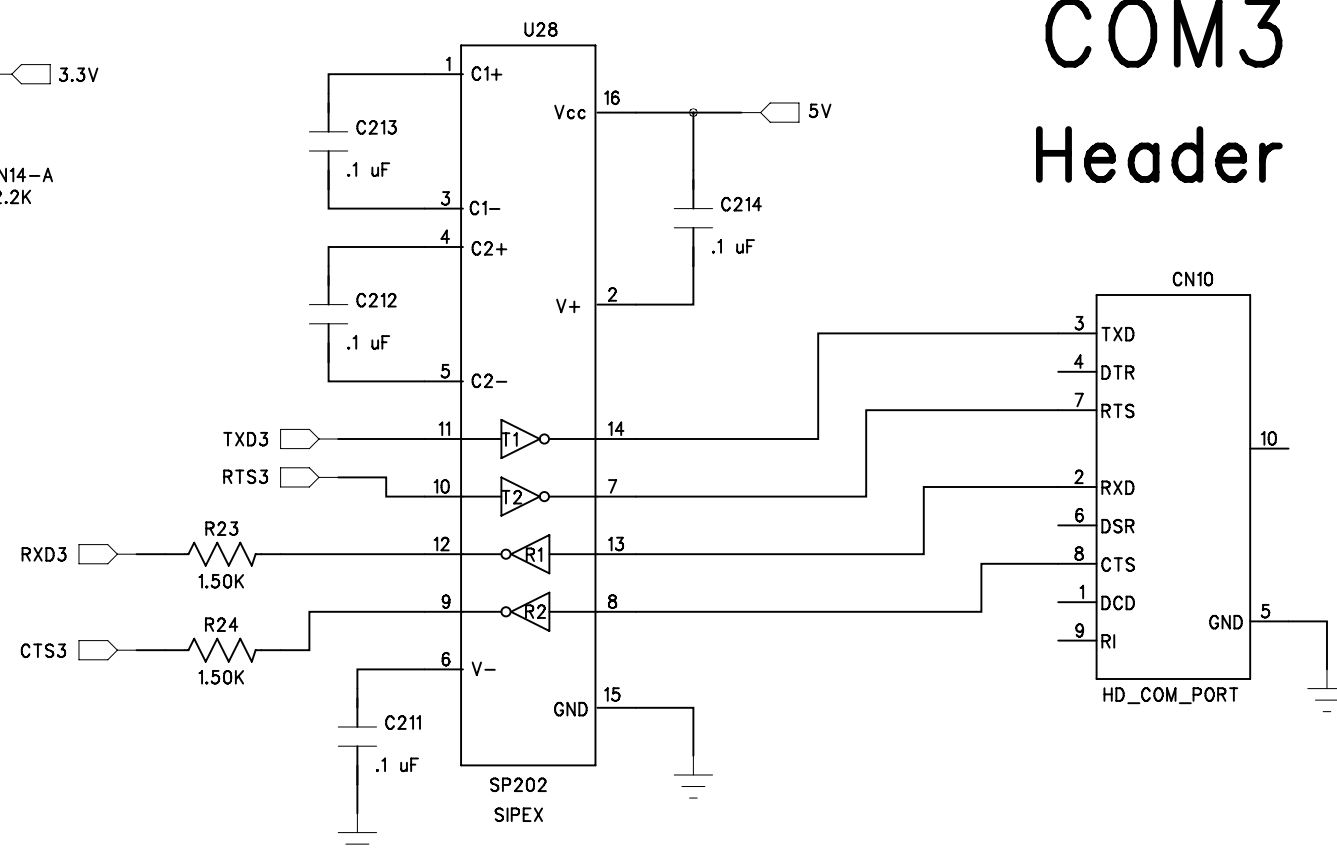
# COM1 RS-232 Transceiver



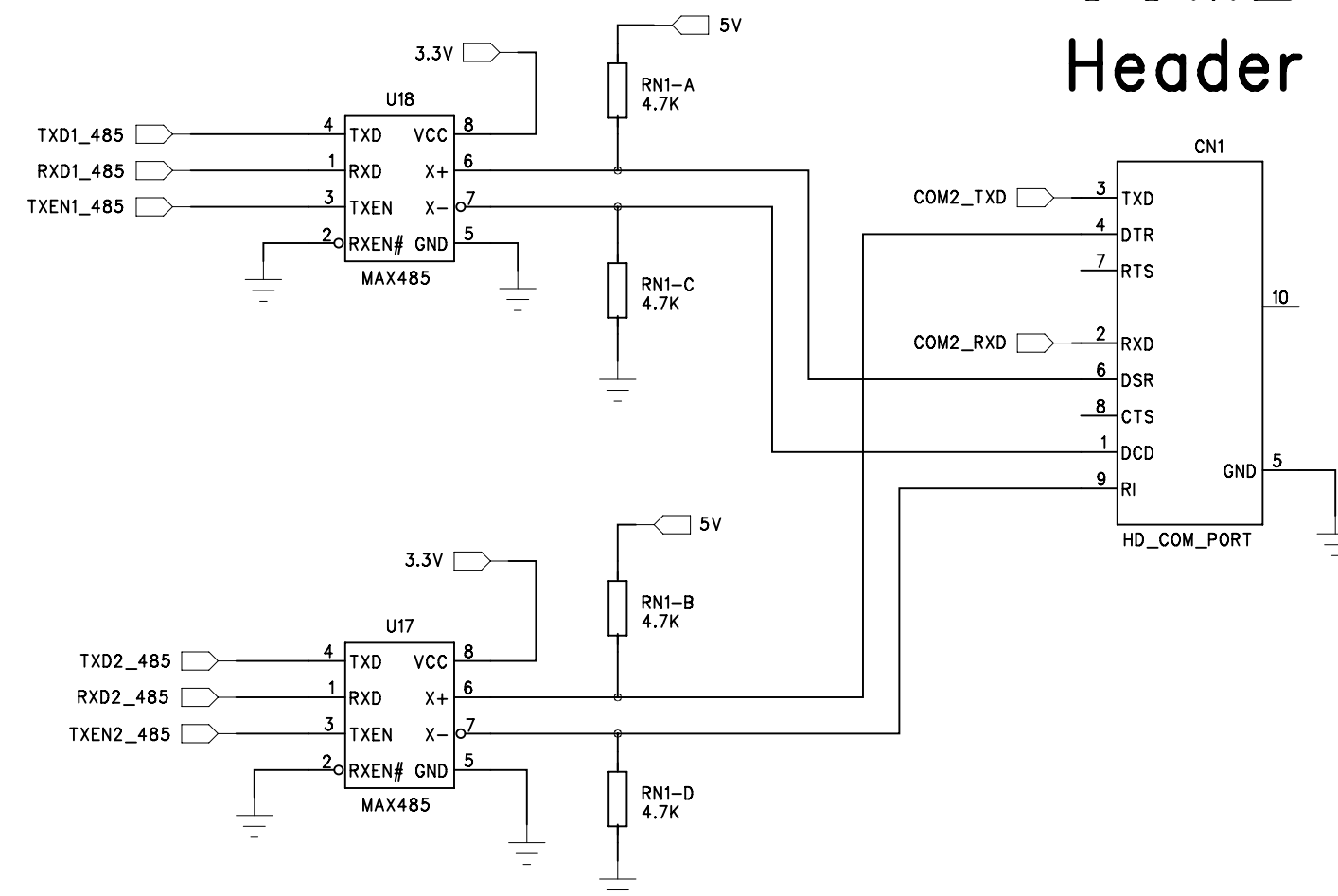
# JTAG Header



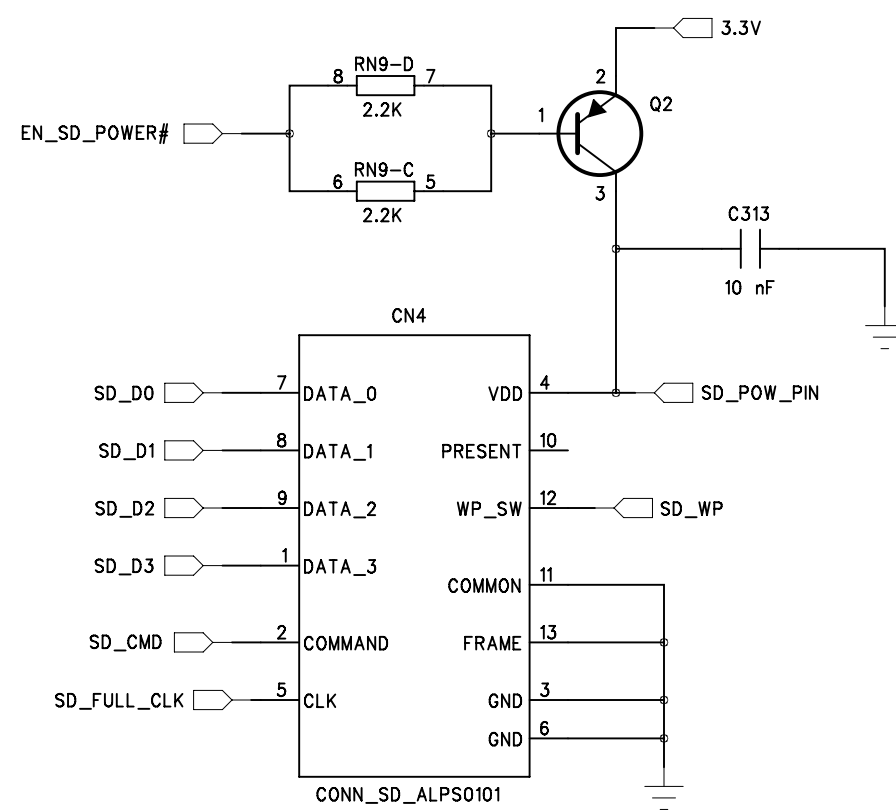
# COM3 Header



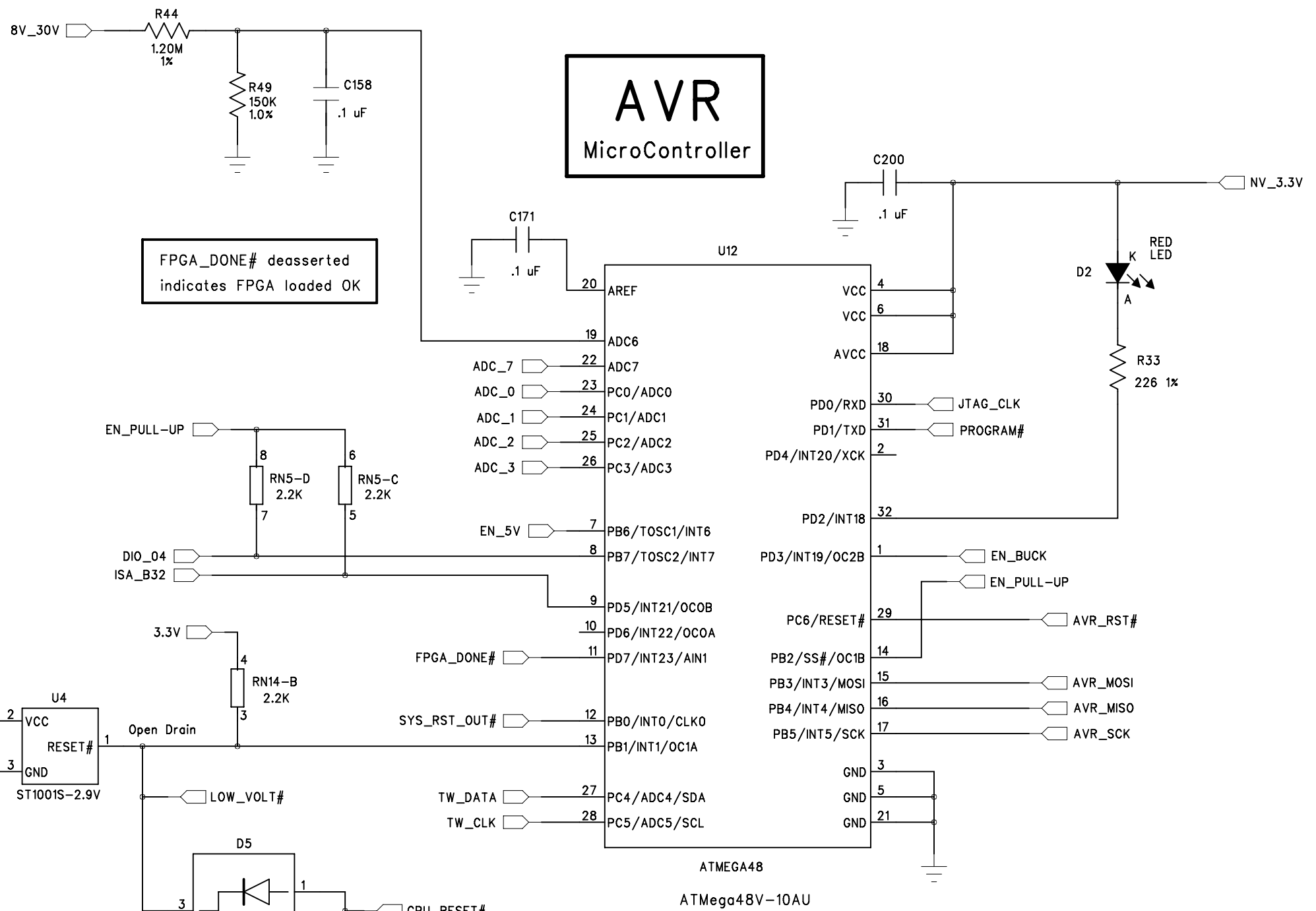
# RS-485 Drivers



# COM2 Header



Must enable pull-up resistors for these pins:  
 SD card D0-D3  
 SD Power#  
 SD card WP



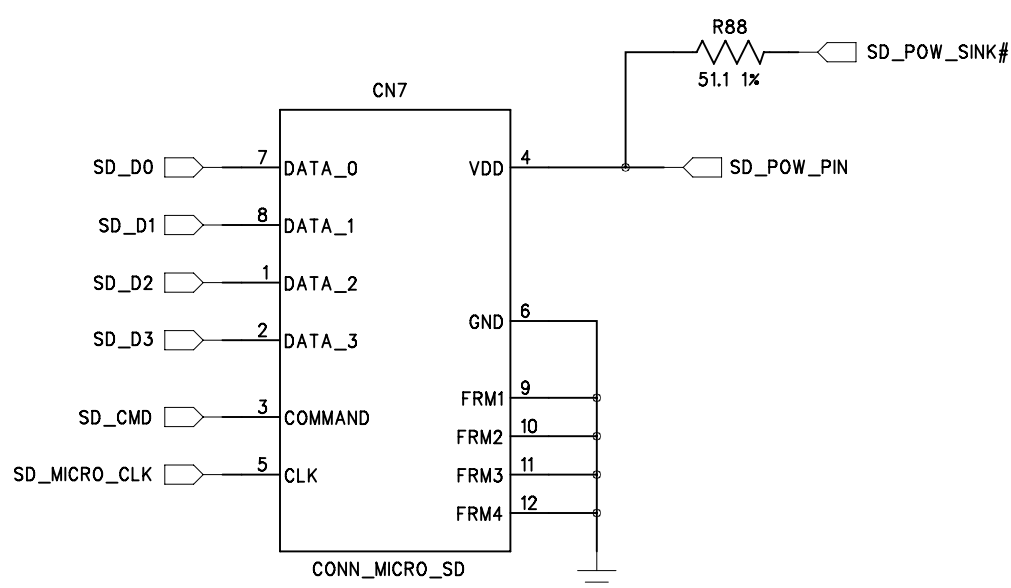
FPGA\_DONE# deasserted indicates FPGA loaded OK

AVR  
 MicroController

Reset will tri-state all pins

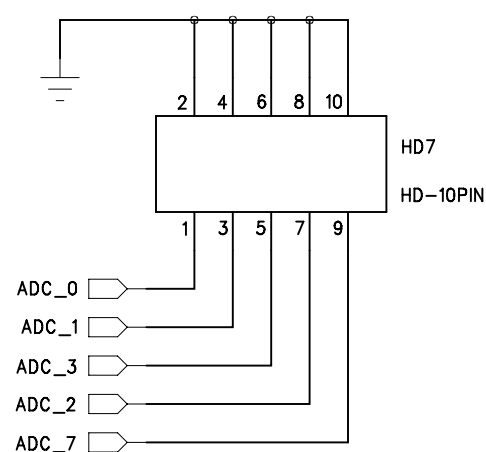
DIO\_04 or ISA\_32 can wake up AVR

### Full-Size SD Card Socket

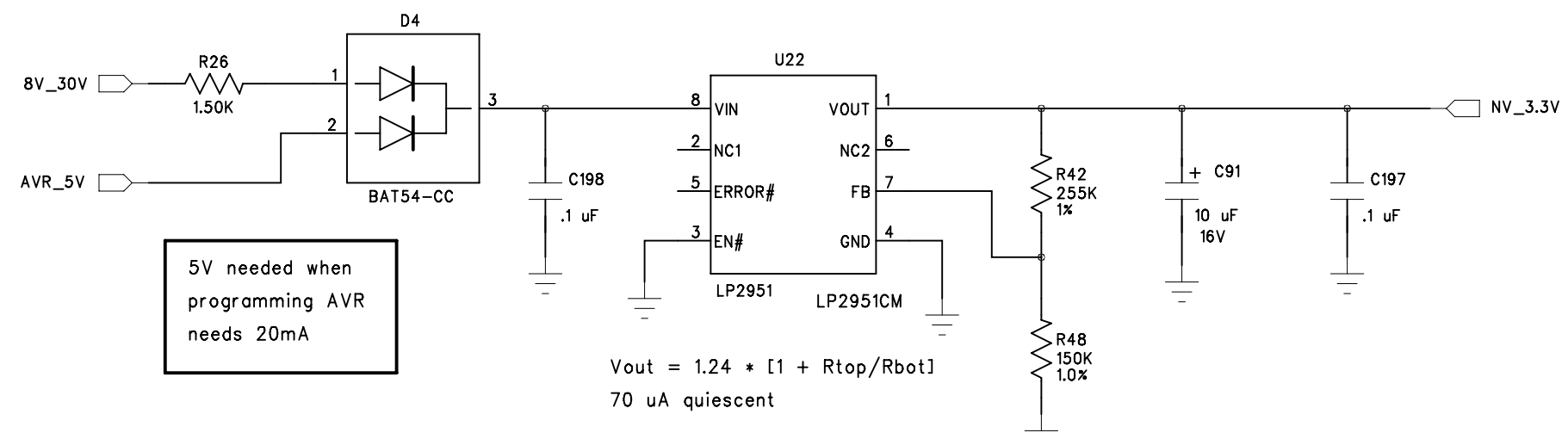


### Micro SD Card Socket

### 5 Channel 10-bit A/D



### NV 3.3V Regulator for AVR

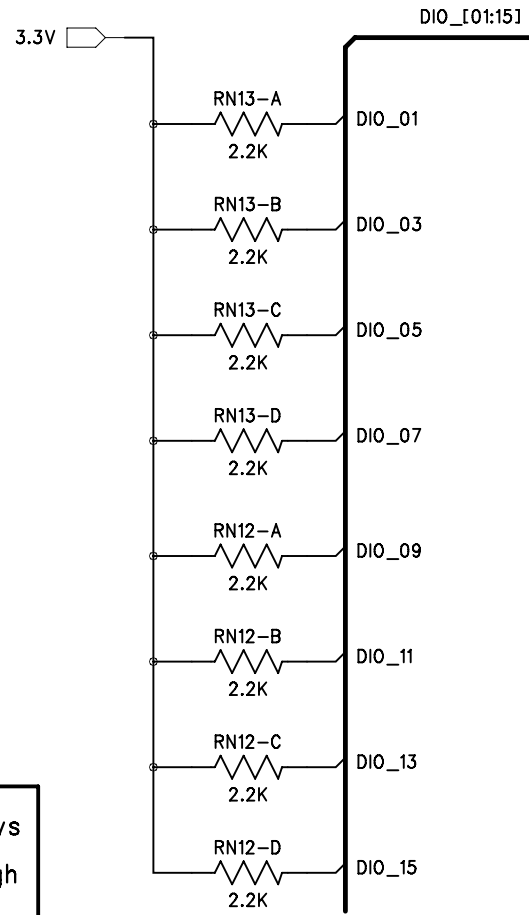
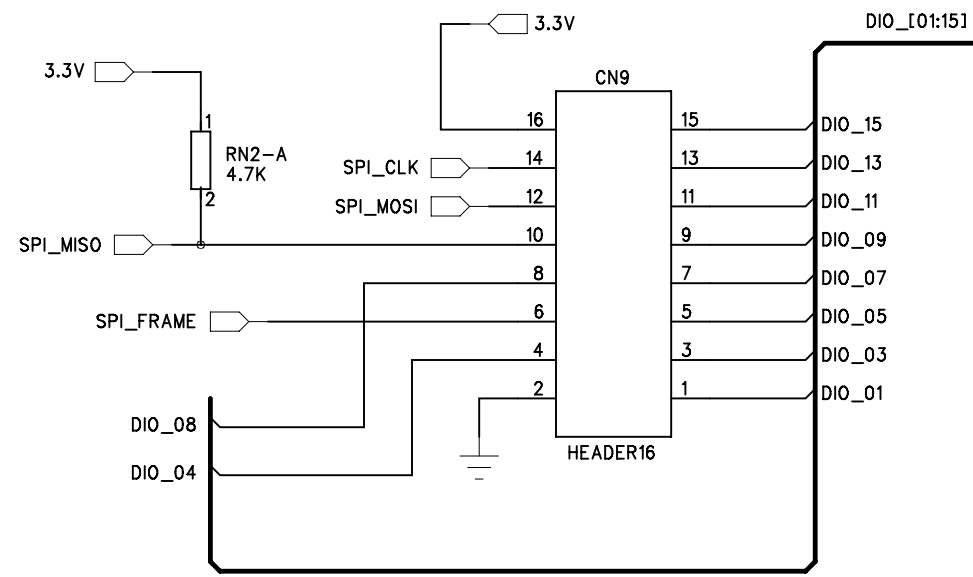


5V needed when programming AVR needs 20mA

$$V_{out} = 1.24 * [1 + R_{top}/R_{bot}]$$

70 uA quiescent

# DIO Port



SPI\_MISO is 5V tolerant  
MOSI, CLK, and Frame  
are 3.3V level outputs

DIO\_01 thru DIO\_15 (odds) are always  
open drain outputs, initialized to high  
They can be used as inputs

DIO\_08 initializes to an input  
when output, active high-low  
It is programmable In or out

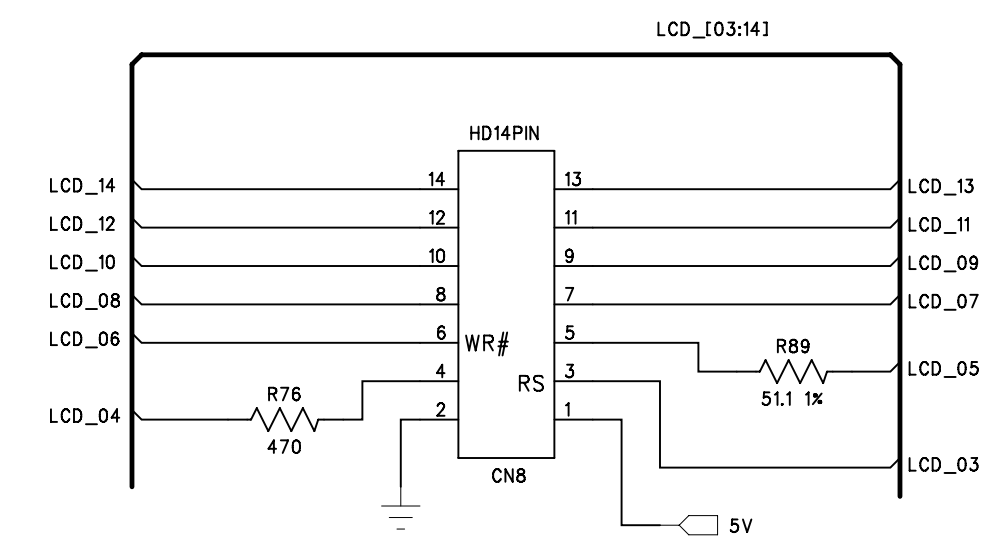
DIO\_04 is always input  
AVR drives pull-up on this pin

Pull-up resistors for  
the open drain outputs

Open drain outputs can  
sink 8 mA, but only source  
current thru resistor

All DIO lines are 5V tolerant

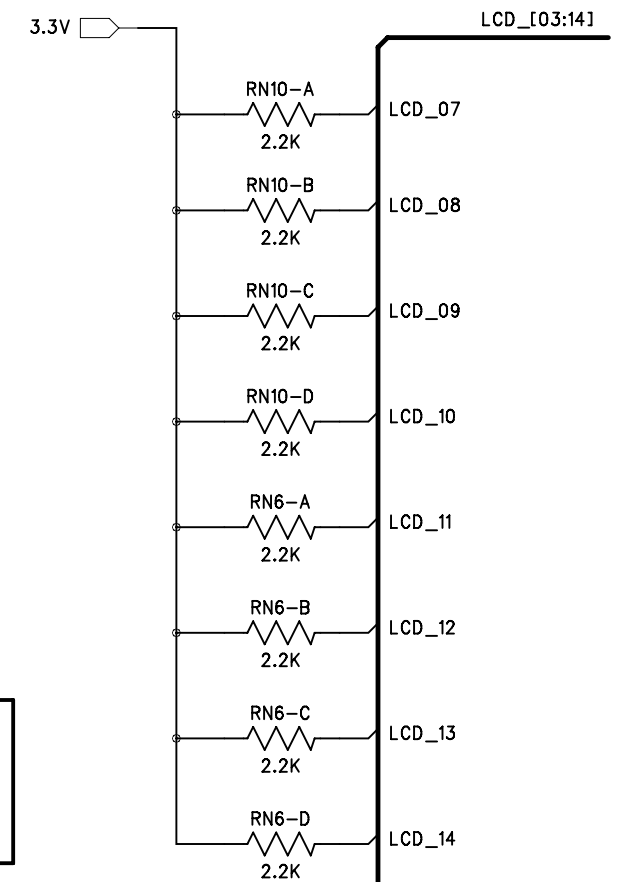
# LCD Port



LCD03, LCD05, LCD06 init to inputs  
when outputs, active high-low  
These are programmable I/O

LCD07 thru LCD14 are always open  
drain outputs, initialized to high  
They can be used as inputs

LCD04 is always output  
active high-low, init to zero

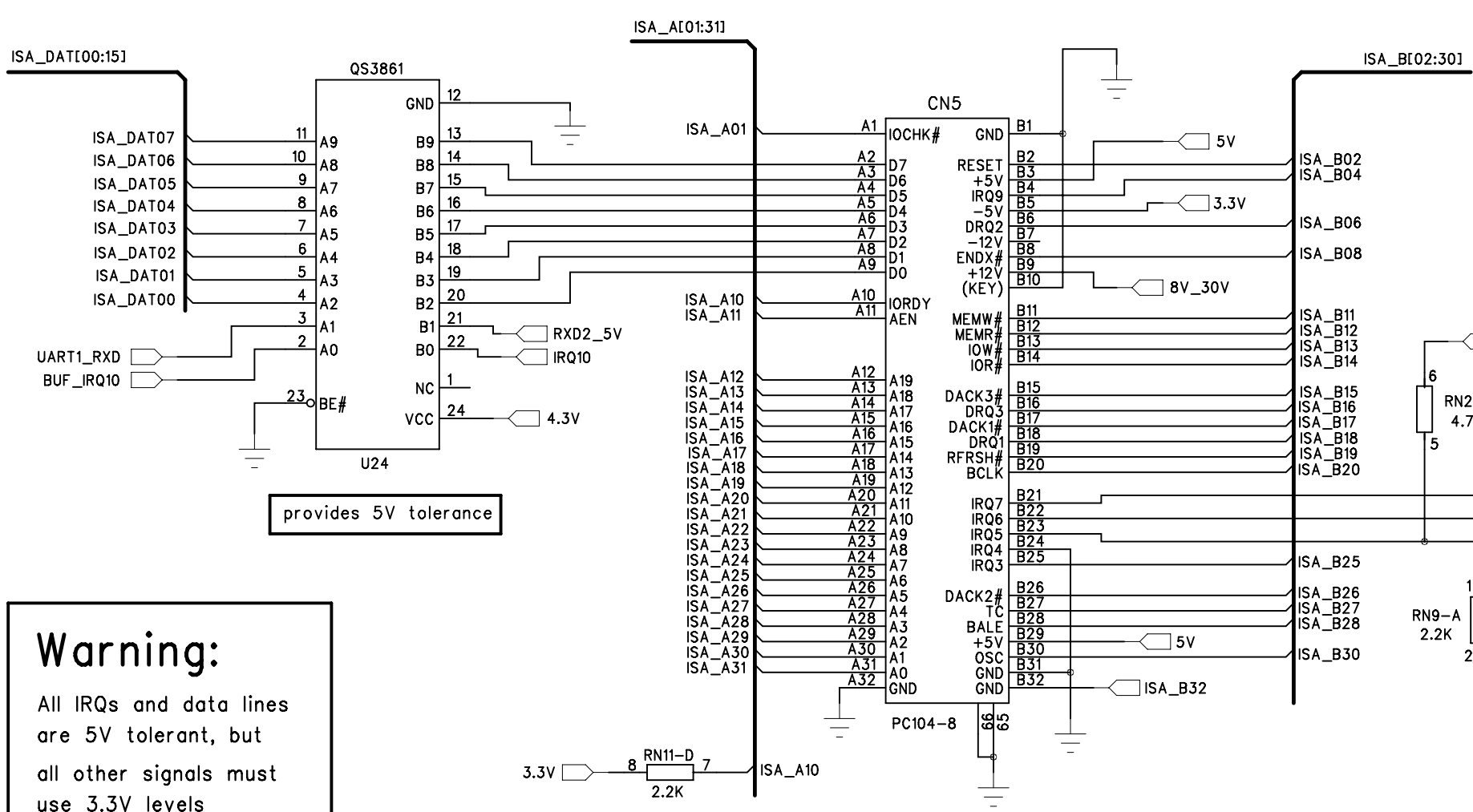


Pull-up resistors for  
the open drain outputs

Open drain outputs can  
sink 8 mA, but only source  
current thru resistor

All LCD lines are 5V tolerant

# PC/104 64-pin Connector

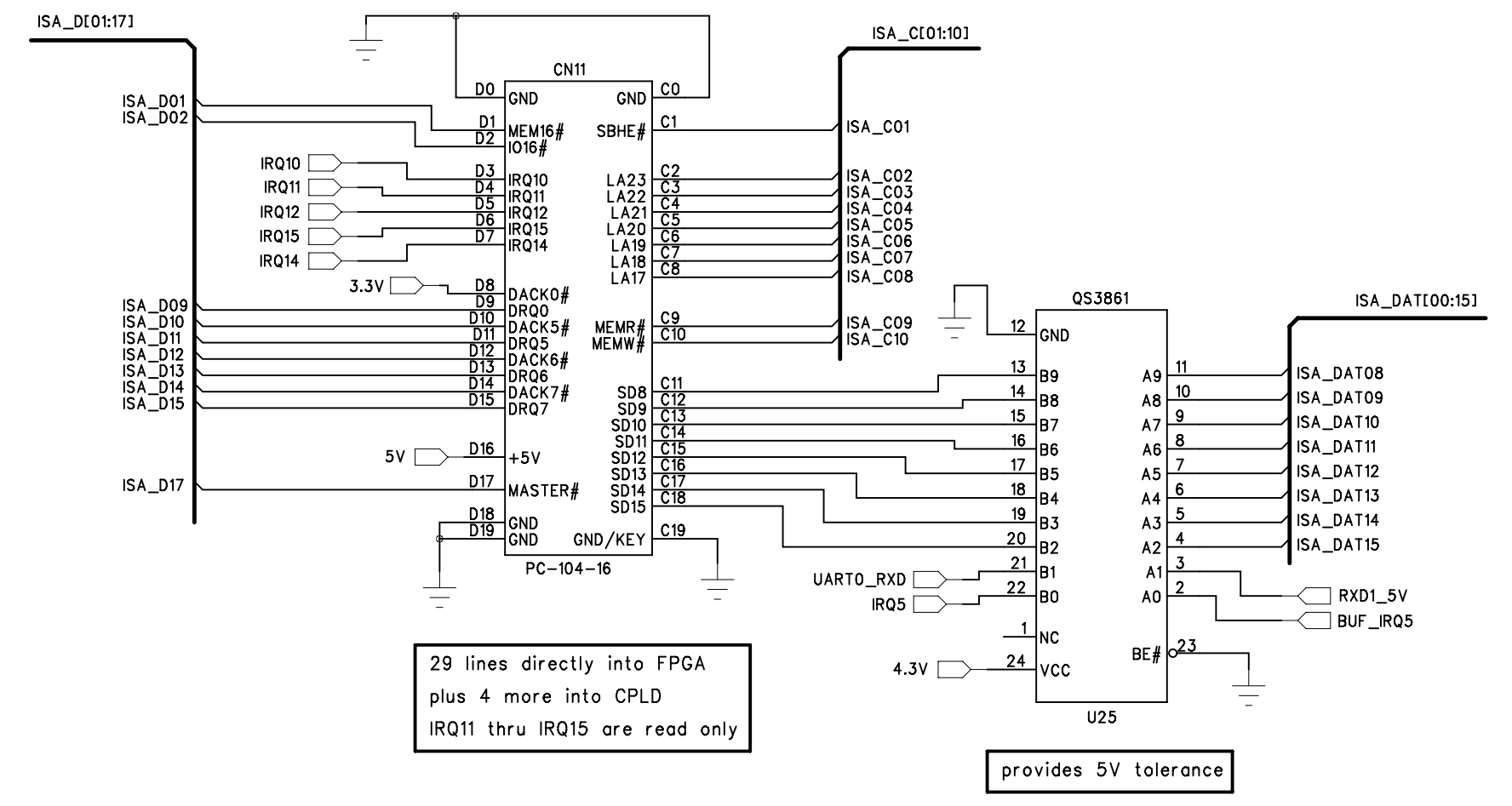


provides 5V tolerance

**Warning:**  
All IRQs and data lines  
are 5V tolerant, but  
all other signals must  
use 3.3V levels  
IRQ3 must be 3.3V levels

51 lines directly into FPGA  
plus 3 more into CPLD (read only)  
(IRQ6, IRQ7 and ISA\_32)

# PC/104 40-pin Connector



29 lines directly into FPGA  
plus 4 more into CPLD  
IRQ11 thru IRQ15 are read only

provides 5V tolerance